

QN7002

N-CHANNEL MOSFET FOR SWITCHING

R07DS0269EJ0100 Rev.1.00 Mar 11, 2011

Description

The QN7002, N-channel vertical type MOSFET designed for general-purpose switch, is a device which can be driven directly by a 4.5 V power source.

Features

- Directly driven by a 4.5 V power source.
- Low on-state resistance

 $R_{DS(on)1} = 2.7 \Omega MAX. (V_{GS} = 10 V, I_{D} = 100 mA)$

 $R_{DS(on)2}$ = 3.2 Ω MAX. (V_{GS} = 4.5 V, I_D = 50 mA)

Ordering Information

Part Number	Lead Plating	Packing	Package
QN7002-T1B-AT	Pure Sn	3000p/Reel	SC-59 (Mini Mold)

Remark "-AT" indicates Pb-free. This product does not contain Pb in external electrode and other parts.

Remark for Agent

ORDER NUMBER "2SK4079(1)" must be used to order, instead of "QN7002". For instance, "2SK4079(1)-T1B-AT"

Absolute Maximum Ratings (TA = 25°C)

Drain to Source Voltage (V _{GS} = 0 V)	VDSS	60	V
Gate to Source Voltage (V _{DS} = 0 V)	V _{GSS}	±20	V
Drain Current (DC)	I _{D(DC)}	200	mA
Drain Current (pulse) Note	I _{D(pulse)}	±800	mA
Total Power Dissipation	Рт	200	mW
Channel Temperature	Tch	150	°C
Storage Temperature	T _{stg}	-55 to +150	°C

Note PW \leq 10 μ s, Duty Cycle \leq 1%

Caution This product is electrostatic-sensitive device due to low ESD capability and should be handled with caution for electrostatic discharge.

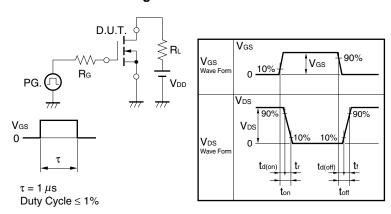
VESD ± 400 V (MIL STD; C = 100 pF, R = 1.5 k Ω , 5 times), as reference value.

Electrical Characteristics (T_A = 25°C)

Characteristics	Symbol	Test Conditions	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	IDSS	V _{DS} = 60 V, V _{GS} = 0 V			1	μА
Gate Leakage Current	Igss	V _{GS} = ±20 V, V _{DS} = 0 V			±10	μΑ
Gate Threshold Voltage	$V_{\text{GS(th)}}$	$V_{DS} = V_{GS}, I_D = 250 \mu A$	1.0		2.5	V
Forward Transfer Admittance Note	y _{fs}	V _{DS} = 10 V, I _D = 100 mA	150			mS
Drain to Source On-state Resistance Note	R _{DS(on)1}	V _{GS} = 10 V, I _D = 100 mA		2.1	2.7	Ω
	R _{DS(on)2}	V _{GS} = 4.5 V, I _D = 50 mA		2.4	3.2	Ω
Input Capacitance	Ciss	V _{DS} = 10 V,		20		pF
Output Capacitance	Coss	V _{GS} = 0 V,		9		pF
Reverse Transfer Capacitance	Crss	f = 1.0 MHz		2		pF
Turn-on Delay Time	t _{d(on)}	V _{DD} = 10 V,		16		ns
Rise Time	t r	I _D = 200 mA,		6.5		ns
Turn-off Delay Time	t _{d(off)}	V _{GS} = 10 V,		82		ns
Fall Time	t _f	R _G = 10 Ω		32		ns
Total Gate Charge	Q _G	I _D = 200 mA, V _{DD} = 25 V, V _{GS} = 10 V		2		nC
Body Diode Forward Voltage Note	V _{F(S-D)}	I _F = 200 mA, V _{GS} = 0 V		0.86		V

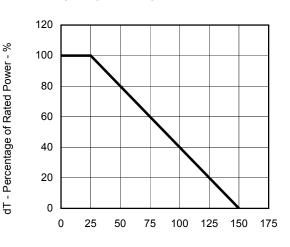
Note Pulsed

Test Circuit Switching Time



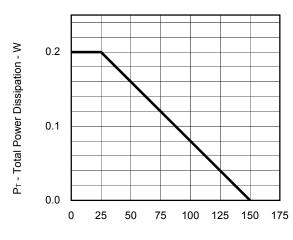
Typical Characteristics (T_A = 25°C)

DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



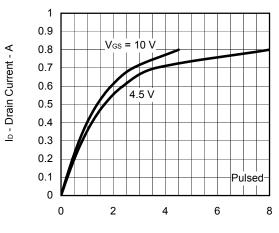
T_A - Ambient Temperature - °C

TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



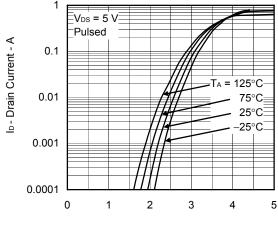
T_A - Ambient Temperature - °C

DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



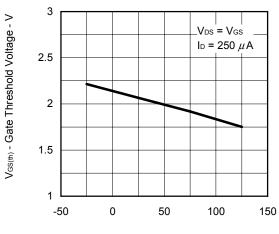
V_{DS} - Drain to Source Voltage - V

FORWARD TRANSFER CHARACTERISTICS



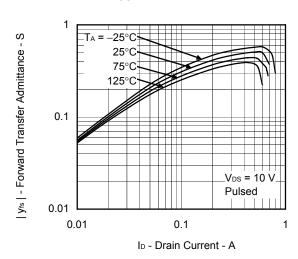
V_{GS} - Gate to Source Voltage - V

GATE THRESHOLD VOLTAGE vs. CHANNEL TEMPERATURE



Tch - Channel Temperature - °C

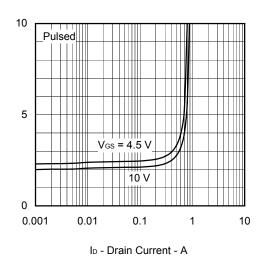
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



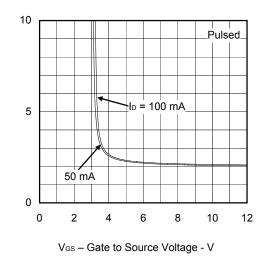
 $\mathsf{R}_{\mathsf{DS}(\mathsf{on})}$ - Drain to Source On-state Resistance - Ω

 $\mathsf{R}_{\mathsf{DS}(\mathsf{on})}\text{-}$ Drain to Source On-state Resistance - Ω

DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT

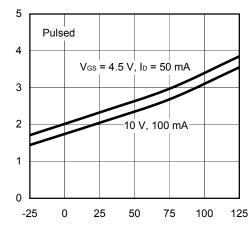


DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

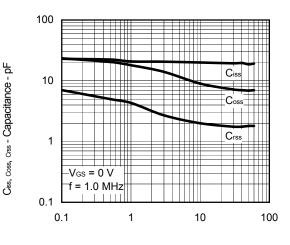


 $\mathsf{R}_{\mathsf{DS}(\mathsf{on})}$ - Drain to Source On-state Resistance - Ω

DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



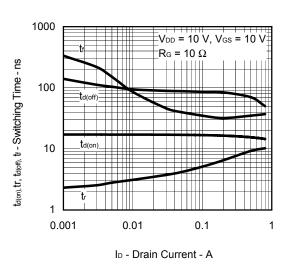
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



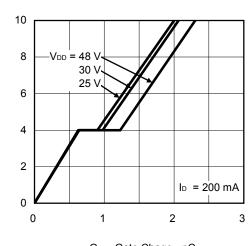
Tch - Channel Temperature - °C

V_{DS} - Drain to Source Voltage - V

SWITCHING CHARACTERISTICS

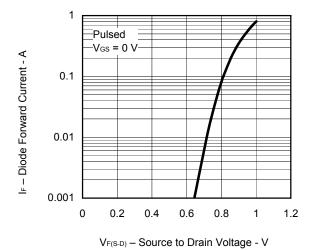


DYNAMIC INPUT CHARACTERISTICS



V_{cs} – Gate to Source Voltage - V

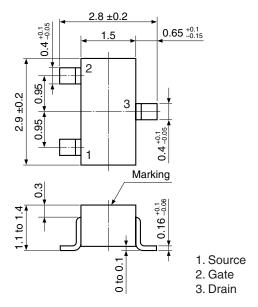
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



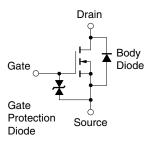
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Package Drawings (Unit: mm)

SC-59 (Mini Mold)



Equivalent Circuit



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

Revision History

QN7002 Data Sheet

		Description		
Rev.	Date	Page	Summary	
1.00	Mar 11, 2011	_	First Edition Issued	

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