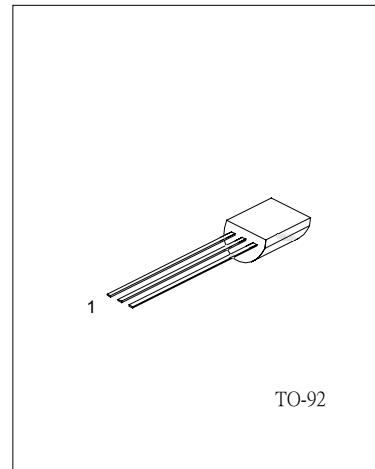


SCRs

DESCRIPTION

Passivated, sensitive gate thyristors in a plastic envelope, intended for use in general purpose switching and phase control applications. These devices are intended to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.



1:CATHODE 2:GATE 3:ANODE

QUICK REFERENCE DATA

PARAMETER	SYMBOL	BT169B	BT169D	BT169E	BT169G	UNIT
		MAX	MAX	MAX	MAX	MAX
Repetitive peak off-state voltages	V_{DRM}, V_{RRM}	200	400	500	600	V
Average on-state current	$I_T(AV)$	0.5	0.5	0.5	0.5	A
RMS on-state current	$I_T(RMS)$	0.8	0.8	0.8	0.8	A
Non-repetitive peak on-state current	I_{TSM}	8	8	8	8	A

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATINGS	UNIT
Repetitive peak off-state voltages	V_{DRM}, V_{RRM}		
BT169B		200*	
BT169D		400*	
BT169E		500*	
BT169G		600*	V
Average on-state current (Half sine wave, $T_{lead} \leq 83^\circ C$)	$I_T(AV)$	0.5	A
RMS on-state current (All conduction angles)	$I_T(RMS)$	0.8	A
Non-repetitive peak on-state current (half sine wave, $T_j=25^\circ C$ prior to surge)	I_{TSM}		
$t=10ms$		8	
$t=8.3ms$		9	A
I^2t for fusing ($t=10ms$)	I^2t	0.32	A^2S
Repetitive rate of rise of on-state current after triggering ($I_{TM}=2A, I_G=10mA, dI_G/dt=100mA/\mu s$)	dI_T/dt	50	$A/\mu s$

PARAMETER	SYMBOL	RATINGS	UNIT
Peak gate current	IGM	1	A
Peak gate voltage	VGM	5	V
Peak reverse gate voltage	VRGM	5	V
Peak gate power	PGM	2	W
Average gate power (Over any 20 ms period)	PG(AV)	0.1	W
Storage temperature	Tstg	-40~150	°C
Operating junction temperature	Tj	125	°C

*Although not recommended, off-state voltages up to 800V may be applied without damage, but the thyristor may switch to the on-state. The rate of rise of current should not exceed 15A/μs.

THERMAL RESISTANCES

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Thermal resistance junction to lead	Rth j-lead			60	K/W
Thermal resistance junction to ambient (pcb mounted, lead length=4mm)	Rth j-a		150		K/W

STATIC ELECTRICAL CHARACTERISTICS (T_j=25°C unless otherwise stated)

PARAMETER	SYMBOL	TSET CONDITIONS	MIN	TYP	MAX	UNIT
Gate trigger current	IGT	Vd=12V, IT=10 mA, gate open circuit	25		55	μA
Latching current	IL	Vd=12V, IGT=0.5mA, RGK=1kΩ		2	6	mA
Holding current	IH	Vd=12V, IGT=0.5mA, RGK=1kΩ		2	5	mA
On-state voltage	VT	IT=1A		1.2	1.35	V
Gate trigger voltage	VGT	Vd=12V, IT=10mA, gate open circuit Vd=VDRM(max), IT=10mA, Tj=125°C, gate open circuit	0.2	0.5 0.3	0.8	V
Off-state leakage current	ID,IR	Vd=VDRM(max), VR=VRM(max), Tj=125°C, RGK=1kΩ		0.05	0.1	mA

DYNAMIC ELECTRICAL CHARACTERISTICS (T_j=25°C unless otherwise stated)

PARAMETER	SYMBOL	TSET CONDITIONS	MIN	TYP	MAX	UNIT
Critical rate of rise of off-state voltage	dVd/dt	VdM=67% VDRM(max), Tj=125°C, exponential waveform, RGK=1kΩ	500	800		V/μs
Gate controlled turn-on time	t _{gt}	ITM=2A, Vd=VDRM(max), IG=10mA, dIg/dt=0.1A/μs		2		μs
Circuit commutated turn-off time	t _q	Vd=67% VDRM(max), Tj=125°C, ITM=1.6A, VR=35V, dITM/dt=30A/μs, Vd/dt=2V/μs, RGK=1kΩ		100		μs

FIG.1 Maximum on-state dissipation, P_{tot} , versus average on-state current, $IT_{(AV)}$, where a =form factor= $IT_{(RMS)} / IT_{(AV)}$

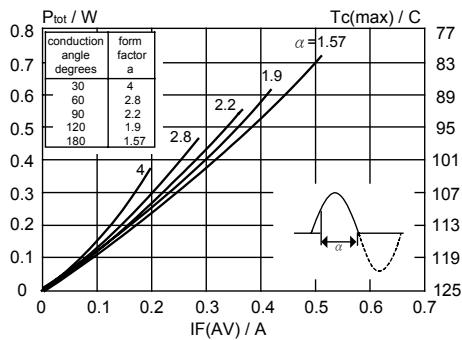


FIG.2 Maximum permissible non-repetitive peak on-state current IT_{SM} , versus pulse width t_p , for sinusoidal currents, $t_p \leq 10ms$.

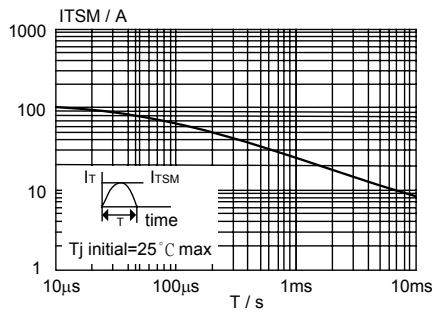


FIG.3 Maximum permissible rms current $IT_{(RMS)}$, versus lead temperature, T_{lead}

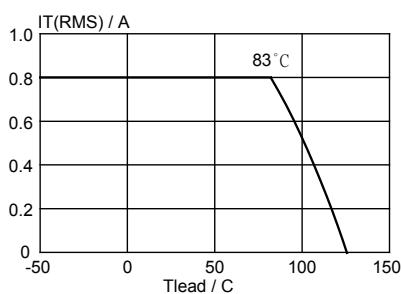


FIG.4 Maximum permissible non-repetitive peak on-state current IT_{SM} , versus number of cycles, for sinusoidal currents, $f = 50Hz$.

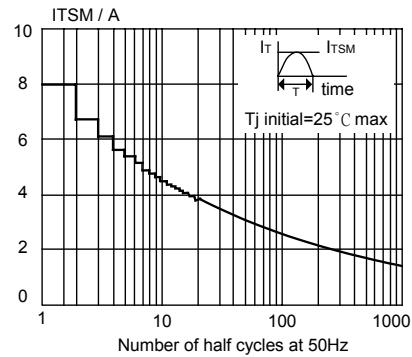


FIG.5 Maximum permissible repetitive rms on-state current $IT_{(RMS)}$, versus surge duration, for sinusoidal currents, $f = 50Hz$; $T_{lead} \leq 83^{\circ}C$

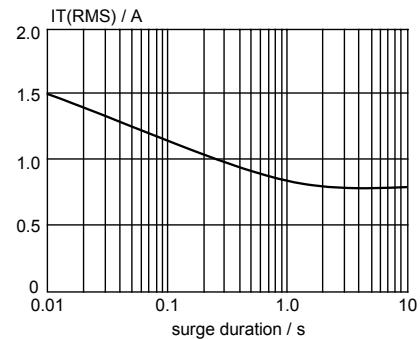


FIG.6 Normalised gate trigger voltage $V_{GT}(T_j) / V_{GT}(25^{\circ}C)$, versus junction temperature T_j

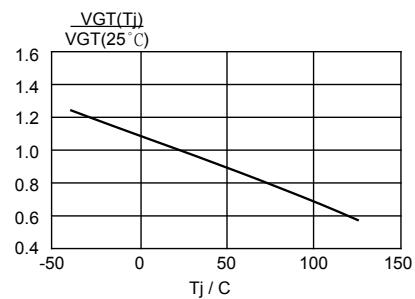


FIG.7 Normalised gate trigger current $I_{GT}(T_j)/I_{GT}(25^\circ C)$, versus junction temperature T_j

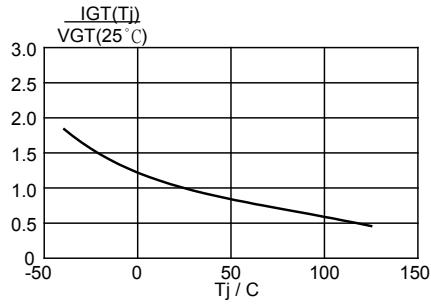


FIG.8 Normalised latching current $I_L(T_j)/I_L(25^\circ C)$, versus junction temperature T_j , $R_{GK}=1\text{ k}\Omega$

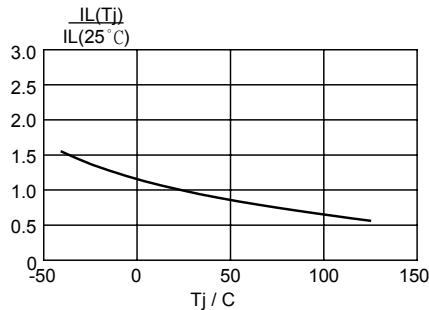


FIG.9 Normalised holding current $I_H(T_j)/I_H(25^\circ C)$, versus junction temperature T_j , $R_{GK}=1\text{ k}\Omega$

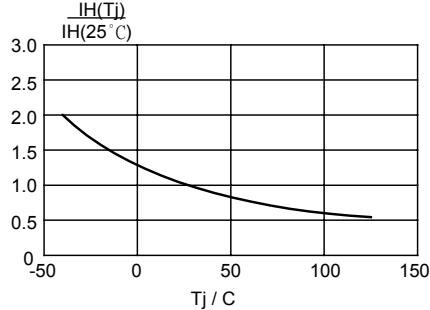


FIG.10 Typical and maximum on-state characteristic.

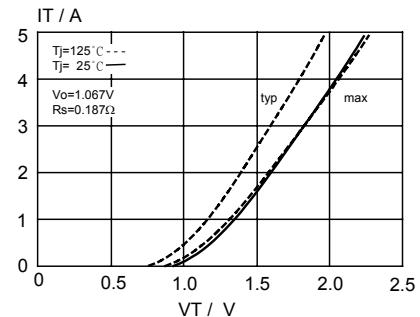


FIG.11 Transient thermal impedance Z_{th} j-lead, versus pulse width t_p .

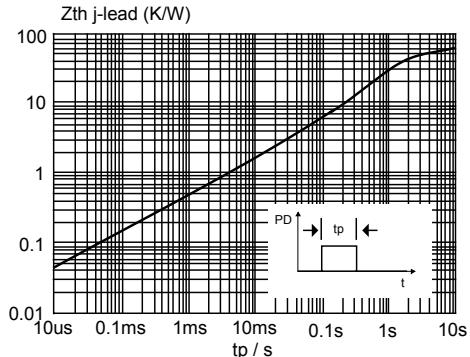
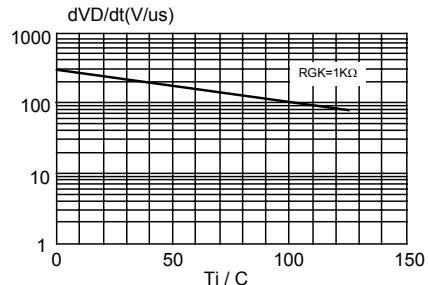


FIG.12 Typical, critical rate of rise of off-state voltage, dV_D/dt versus junction temperature T_j .



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