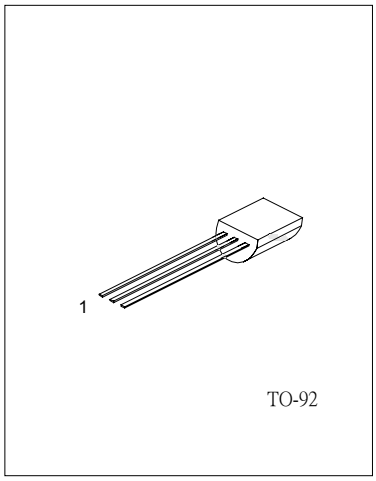
SCRs

DESCRIPTION

Passivated, sensitive gate thyristors in a plastic envelope, intended for use in general purpose switching and phase control applications. These devices are intended to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.



1:CATHODE 2:GATE 3:ANODE

QUICK REFERENCE DATA

PARAMETER	SYMBOL	BT169B	BT169D	BT169E	BT169G	UNIT
		MAX	MAX	MAX	MAX	MAX
Repetitive peak off-state voltages	V_{DRM}, V_{RRM}	200	400	500	600	V
Average on-state current	$I_{T(AV)}$	0.5	0.5	0.5	0.5	A
RMS on-state current	$I_{T(RMS)}$	0.8	0.8	0.8	0.8	A
Non-repetitive peak on-state current	I_{TSM}	8	8	8	8	A

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATINGS	UNIT
Repetitive peak off-state voltages	V_{DRM},V_{RRM}		
BT169B		200*	V
BT169D		400*	
BT169E		500*	
BT169G		600*	
Average on-state current (Half sine wave, Tlead≦83°C)	$I_{T(AV)}$	0.5	A
RMS on-state current (All conduction angles)	$I_{T(RMS)}$	0.8	A
Non-repetitive peak on-state current (half sine wave, Tj=25°C prior to surge)	I_{TSM}		A
t=10ms		8	
t=8.3ms		9	
I^2t for fusing (t=10ms)	I^2t	0.32	A^2S
Repetitive rate of rise of on-state current after triggering (I_{TM}=2A,I_G=10mA, dI_G/dt=100mA/μs)	dI_T/dt	50	A/μs

PARAMETER	SYMBOL	RATINGS	UNIT
Peak gate current	I_{GM}	1	A
Peak gate voltage	V_{GM}	5	V
Peak reverse gate voltage	V_{RGM}	5	V
Peak gate power	P_{GM}	2	W
Average gate power (Over any 20 ms period)	$P_{G(AV)}$	0.1	W
Storage temperature	Tstg	-40~150	°C
Operating junction temperature	Tj	125	°C

*Although not recommended, off-state voltages up to 800V may be applied without damage, but the thyristor may switch to the on-state. The rate of rise of current should not exceed 15A/μs.

THERMAL RESISTANCES

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Thermal resistance junction to lead	Rth j-lead			60	K/W
Thermal resistance junction to ambient (pcb mounted, lead length=4mm)	Rth j-a		150		K/W

STATIC ELECTRICAL CHARACTERISTICS (Tj=25°C unless otherwise stated)

PARAMETER	SYMBOL	TSET CONDITIONS	MIN	TYP	MAX	UNIT
Gate trigger current	I_{GT}	V_D=12V, IT=10 mA, gate open circuit	25		55	μA
Latching current	I_L	V_D=12V, I_{GT}=0.5mA, R_{GK}=1kΩ		2	6	mA
Holding current	I_H	V_D=12V,I_{GT}=0.5mA, R_{GK}=1kΩ		2	5	mA
On-state voltage	V_T	I_T=1A		1.2	1.35	V
Gate trigger voltage	V_{GT}	V_D=12V, I_T=10mA, gate open circuit V_D=$V_{DRM(max)}$, IT=10mA , Tj=125°C, gate open circuit	0.2	0.5 0.3	0.8	V
Off-state leakage current	I_D,I_R	V_D=$V_{DRM(max)}$, V_R=$V_{RRM(max)}$, Tj=125°C, R_{GK}=1kΩ		0.05	0.1	mA

DYNAMIC ELECTRICAL CHARACTERISTICS (Tj=25°C unless otherwise stated)

PARAMETER	SYMBOL	TSET CONDITIONS	MIN	TYP	MAX	UNIT
Ciritical rate of rise of off-state voltage	dV_D/dt	V_{DM}=67% $V_{DRM(max)}$, Tj=125°C, exponential waveform, R_{GK}=1kΩ	500	800		V/μs
Gate controlled turn-on time	t_{gt}	I_{TM}=2A,V_D=V_{DRM}(max), I_G=10mA, dI_G/dt=0.1A/μs		2		μs
Circuit commutated turn-off time	tq	V_D=67% $V_{DRM(max)}$, Tj=125°C, I_{TM}=1.6A,V_R=35V, dI_{TM}/dt=30A/μs, V_D/dt=2V/μs, R_{GK}=1kΩ		100		μs

FIG.1 Maximum on-state dissipation, P_{tot}, versus average on-state current, $I_{T(AV)}$, where a=form factor=$I_{T(RMS)}$ / $I_{T(AV)}$

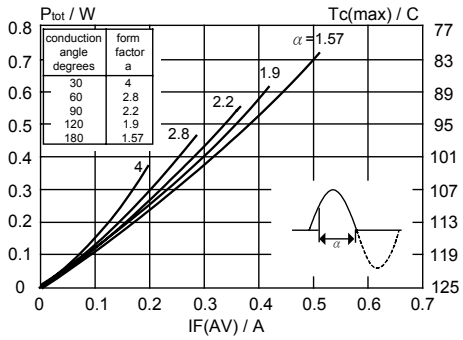


FIG.2 Maximum permissible non-repetitive peak on-state current I_{TSM},versus pulse width tp,for sinusoidal currents, $t_p \leqq 10$ms.

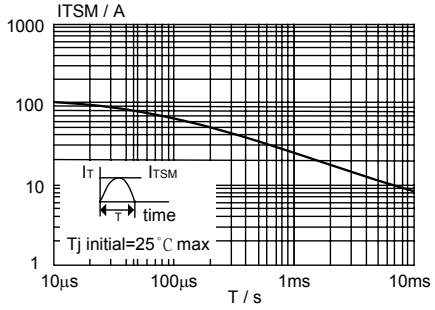


FIG.3 Maximum permissible rms current $I_{T(RMS)}$, versus lead temperature, Tlead

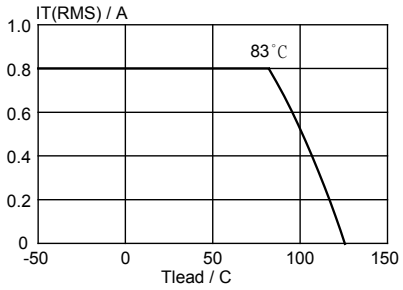


FIG.4 Maximnum permissible non-repetitive peak on-state current I_{TSM}, versus number of cycles, for sinusoidal currents, f = 50Hz.

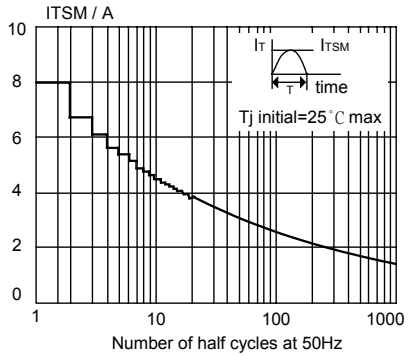


FIG.5 Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f= 50Hz; Tlead$\leqq$83°C

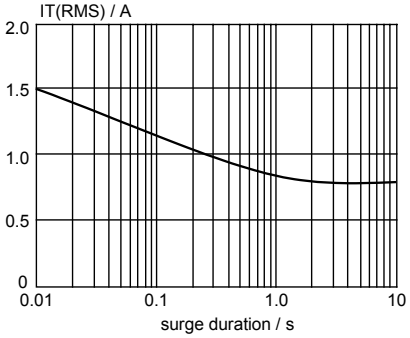


FIG.6 Normalised gate trigger voltage $V_{GT}(Tj)$/ $V_{GT}(25°C)$, versus junction temperature Tj

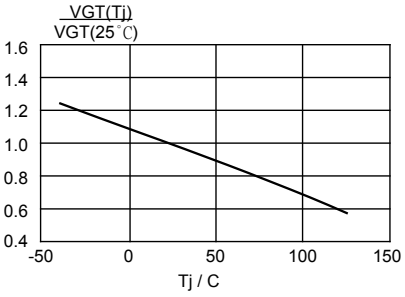


FIG.7 Normalised gate trigger current $I_{GT}(Tj)/I_{GT}(25^{\circ}C)$, versus junction temperature Tj

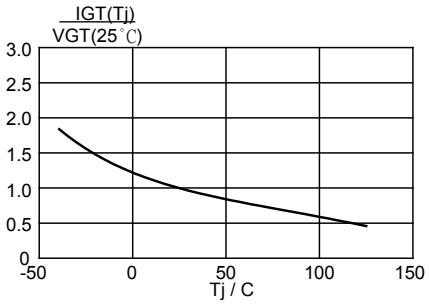


FIG.8 Normalised latching current $I_L(Tj)/I_L(25^{\circ}C)$, versus junction temperature Tj, R_{GK}= 1KΩ

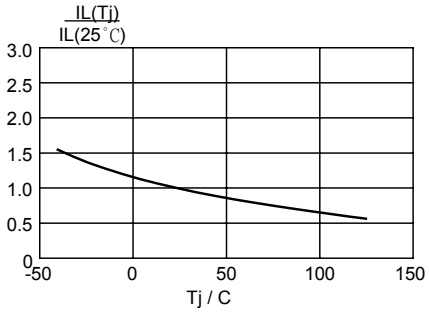


FIG.9 Normalised holding current $I_H(Tj)/I_H(25^{\circ}C)$, versus junction temperature Tj, R_{GK}=1KΩ

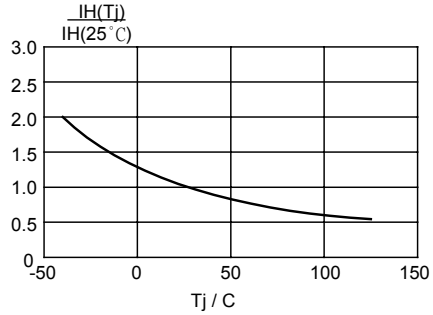


FIG.10 Typical and maximum on-state characteristic.

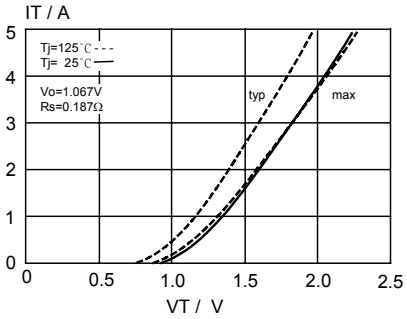


FIG.11 Transient thermal impedance Zth j-lead, versus pulse width tp.

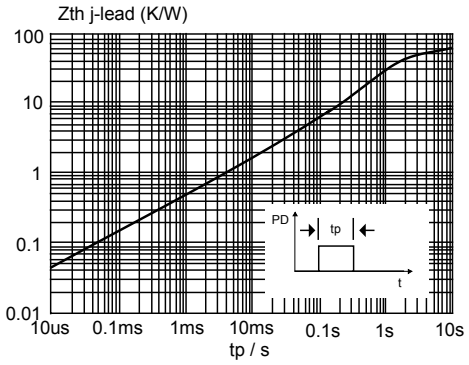


FIG.12 Typical, critical rate of rise of off-state voltage, dV_D/dt versus junction temperature Tj.